GA-M61SME-S2

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23	IDE/FDD/COM/LPT
24	F_USB/ R_USB
25	ALC883 HD-AUDIO

SHEET	TITLE
26	AUDIO JACK, L_OUT, F_AUDIO
27	FRONT PANEL POWER SEQUENCE
28	ATX POWER, VCC12_DUAL, VDDA25
29	PWM ISL6312

Revision: 2.01

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M61SME-S2 | Rev: 2.01

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Model Name:GA-M61SME-S2 Rev.2.01

Component value change history

P-Code: U95044-0

Date	Change Item	Reason
2007.01.18	2.0A E_BOM issue PCB:2.0	New BOM release
		IO change to IT8716/GB/CX PCIE x16 change to blue
2007.02.13	2.0B P_BOM issue PCB:2.01	PVT
2007.03.09	2.0B ECN issue PCB:2.01	Add new source10CM1-022203-56R

Circuit or PCB layout change for next version

Date	Change Item	Reason
2007.01.17	2.0 Gerber Out	Modify from M61VME-S2 2.01
2007.02.07	2.01 Gerber Out	PCI_E change to x8, Change Choke foot print. Add F_USB 0805 by pass CAP

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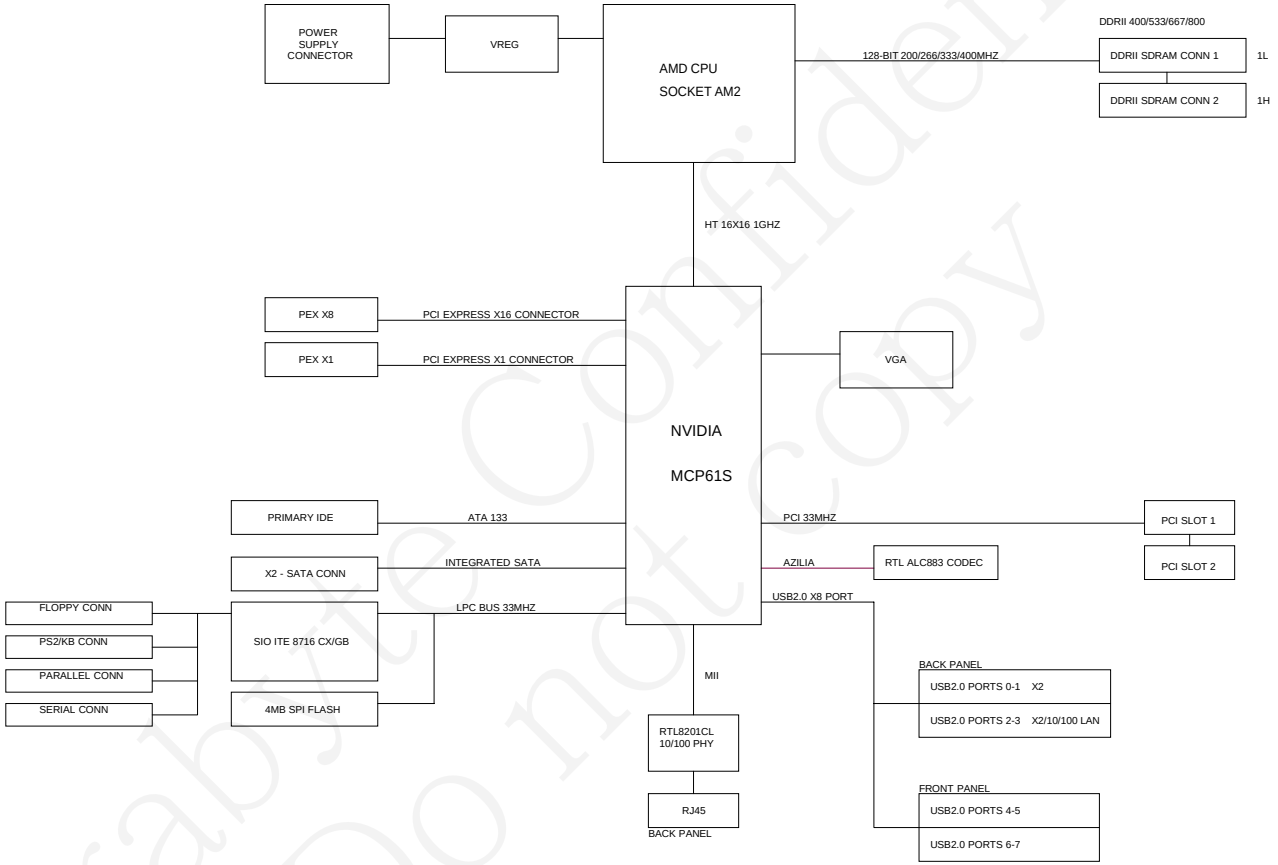
Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M61SME-S2 | Rev: 2.01

Date: Friday, March 09, 2007 | Sheet 2 of 29

BLOCK DIAGRAM



GIGABYTE		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M61SME-S2	Rev: 2.01
Date: Thursday, March 08, 2007	Sheet 3 of 29	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

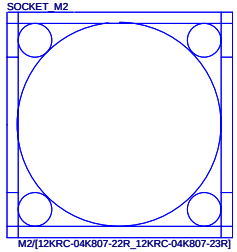
M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
				Y6	1 TP78
				W6	1 TP79
L0_CTLIN_H0	U1	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	W2	L0_CTLOUT_H0 <11>
L0_CTLIN_L0	V1	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W3	L0_CTLOUT_L0 <11>
		L0_CTLIN_H(0)	L0_CTLOUT_H(0)		
		L0_CTLIN_L(0)	L0_CTLOUT_L(0)		
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

VCC12_HT — R3 49.9/4/1 — V4
GND — R4 49.9/4/1 — V5

SOCKET_M2



M2/[12KRC-04K807-22R_12KRC-04K807-23R]

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Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
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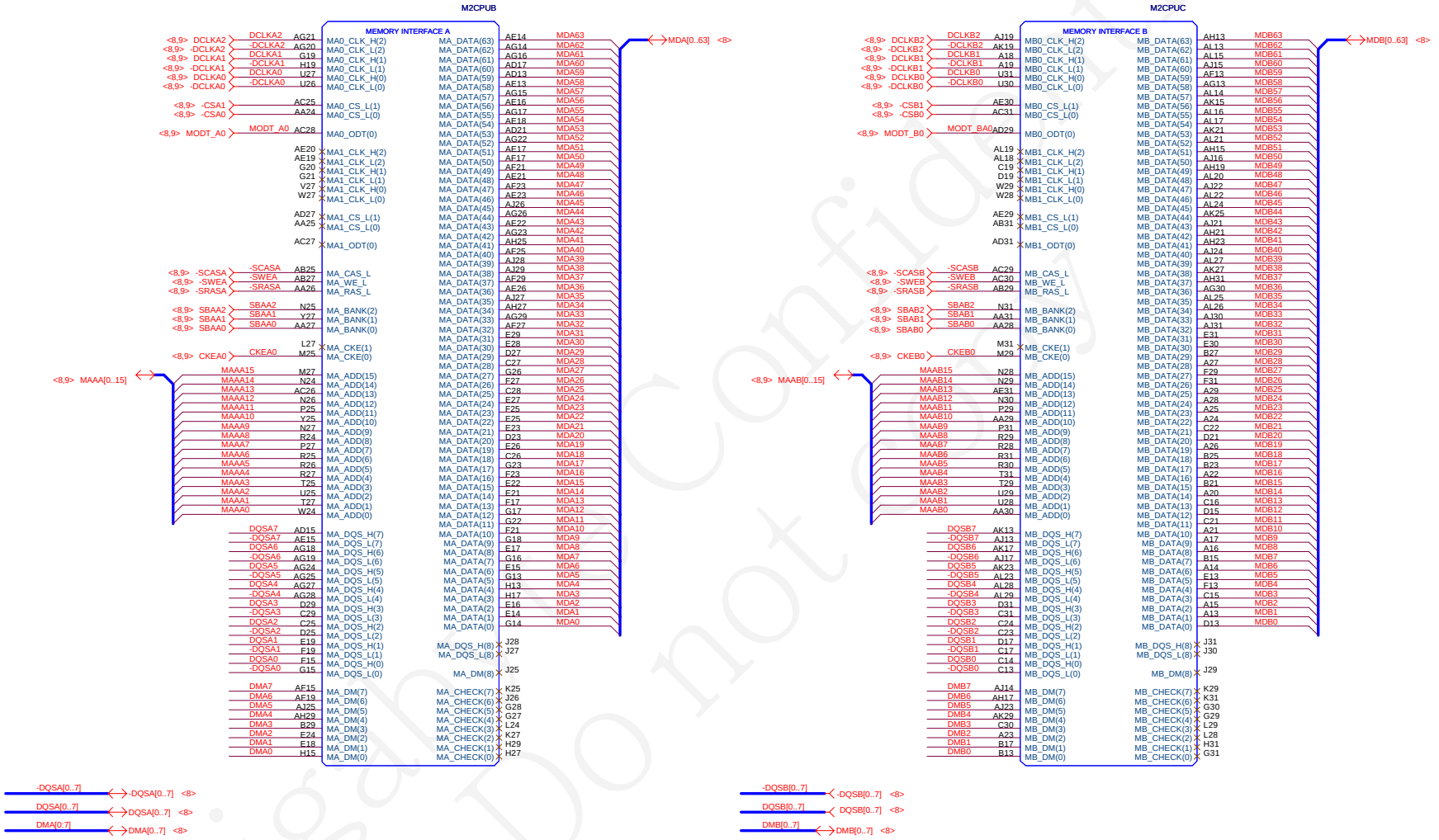

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Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-M61SME-S2	Rev: 2.01
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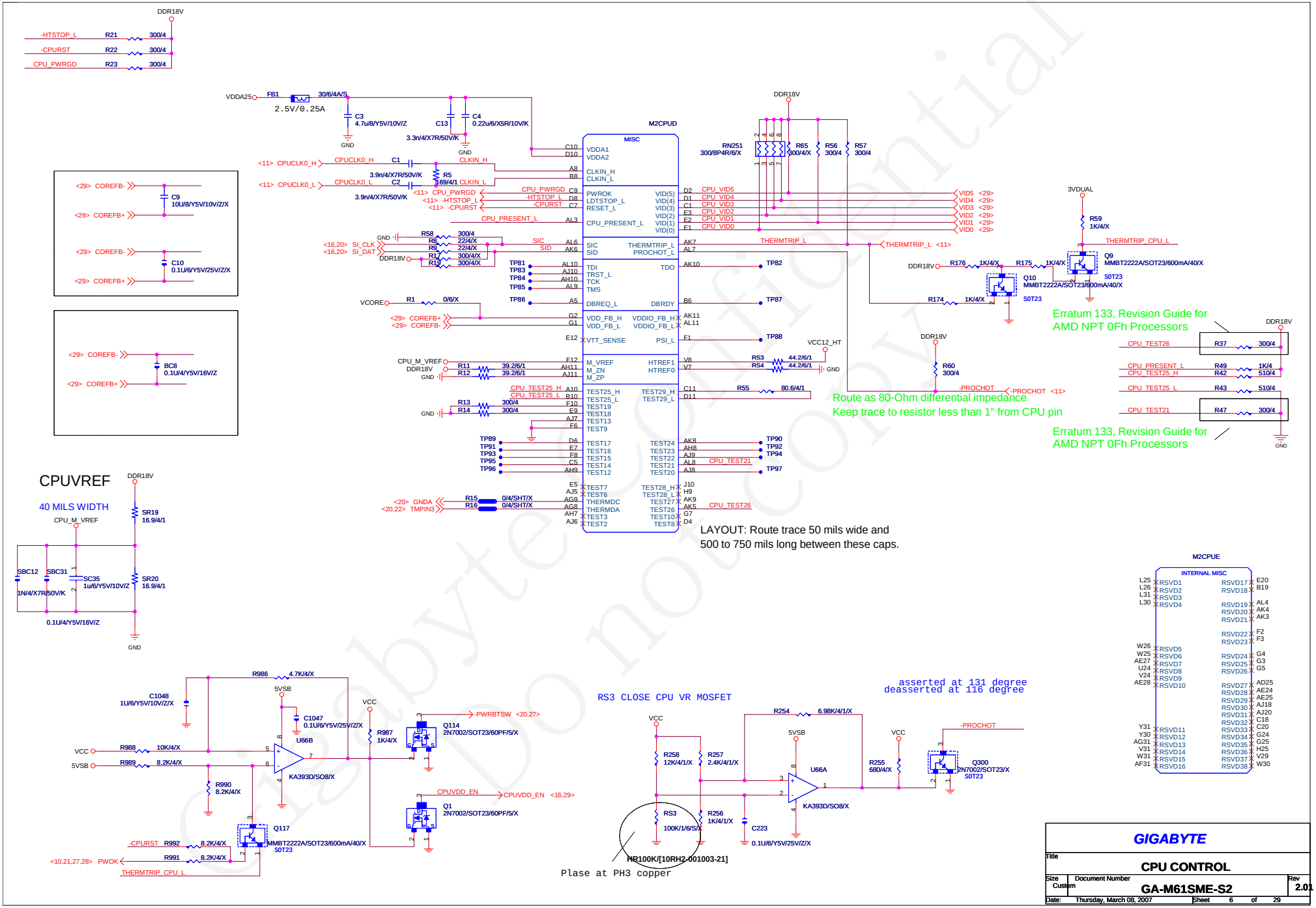
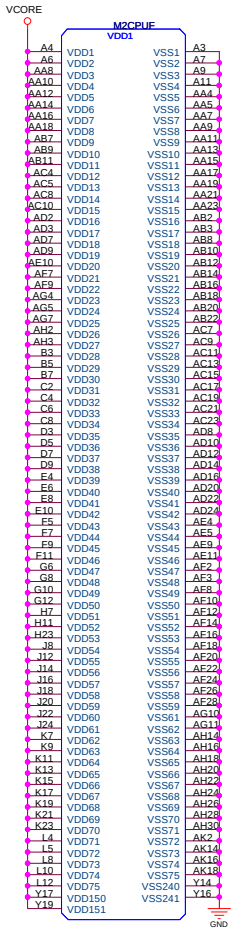
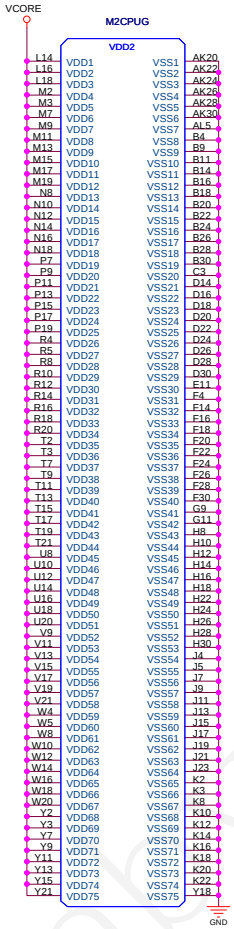
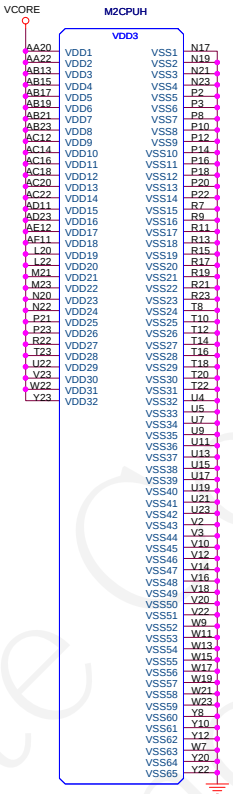
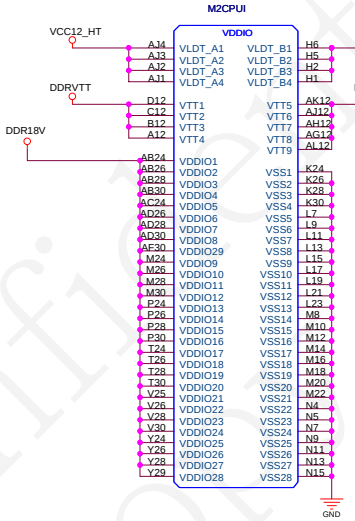


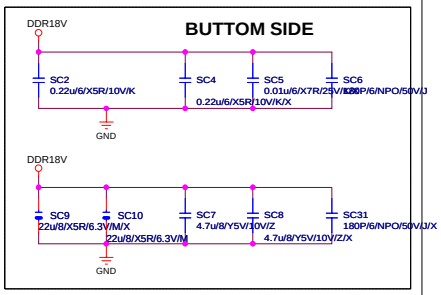
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

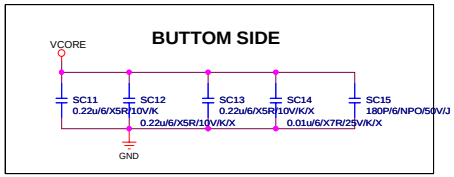


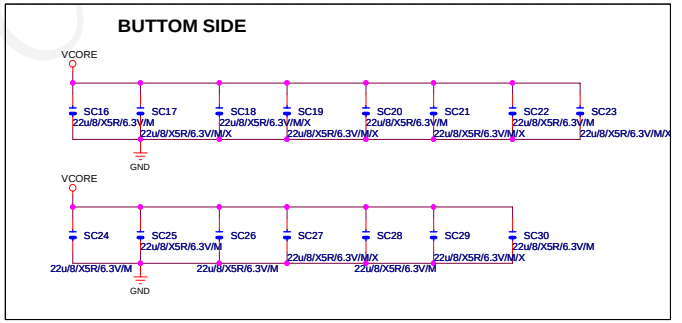


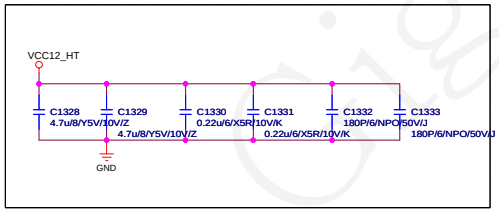


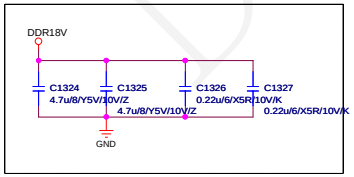


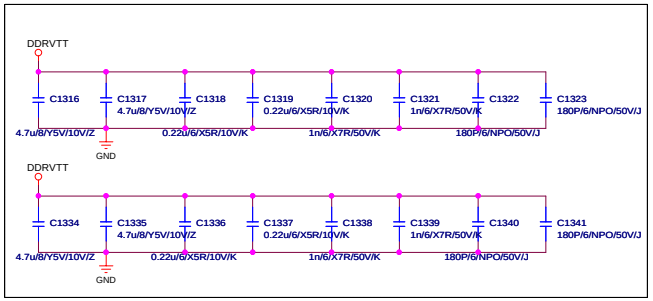


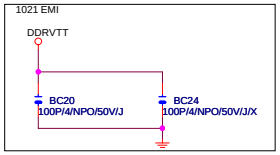












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Title: CPU POWER & GND

Size	Document Number	Rev
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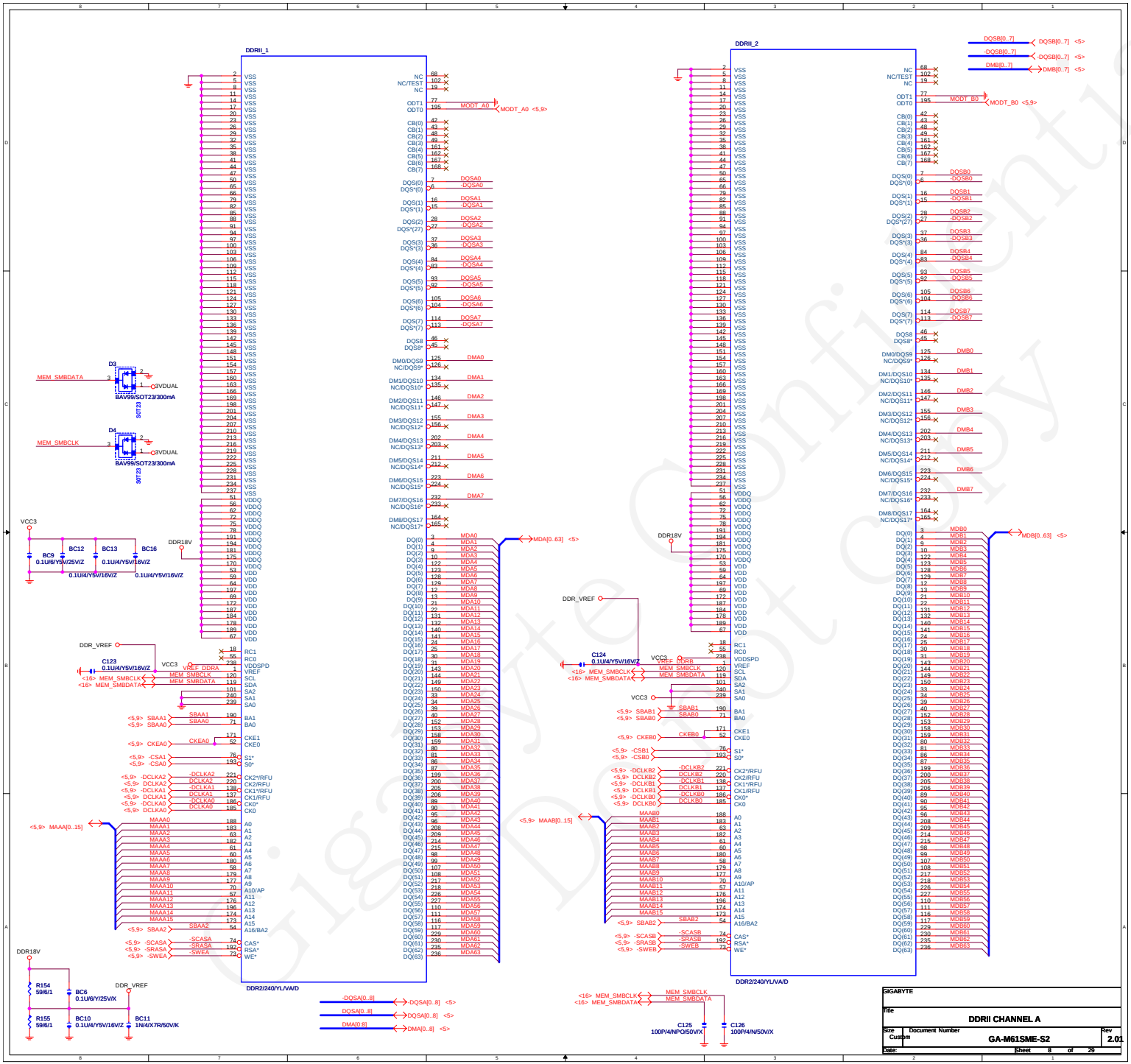
DDRII_1
DDRII_2
DDR2/240/YL/VA/D
DDR2/240/YL/VA/D
MEM_SMBDATA
MEM_SMBCLK
D3
D4
BAV99/SOT23/300mA
SOT23
3VDUAL
VCC3
DDR18V
DDR_VREF
BC9 0.1U/6/Y5V/25V/Z
BC12
BC13 0.1U/4/Y5V/16V/Z
BC16
0.1U/4/Y5V/16V/Z
C123 0.1U/4/Y5V/16V/Z
C124 0.1U/4/Y5V/16V/Z
C125 100P/4/NP0/50V/X
C126 100P/4/N/50V/X
R154 59/6/1
R155 59/6/1
BC6 0.1U/6/Y/25V/X
BC10 0.1U/4/Y5V/16V/Z
BC11 1N/4/X7R/50V/K
DQSB[0..7]
-DQSB[0..7]
DMB[0..7]
MODT_B0
MDB[0..63]
DQSA[0..8]
-DQSA[0..8]
DMA[0..8]
MODT_A0
MDA[0..63]
MAAB[0..15]
MAAA[0..15]
SBAB1
SBAB0
SBAA1
SBAA0
CKEB0
CKEA0
CSB1
CSB0
CSA1
CSA0
DCLKB2
-DCLKB2
DCLKB1
-DCLKB1
DCLKB0
-DCLKB0
DCLKA2
-DCLKA2
DCLKA1
-DCLKA1
DCLKA0
-DCLKA0
SBAB2
SBAA2
SCASB
SRASB
SWEB
SCASA
SRASA
SWEA
MEM_SMBCLK
MEM_SMBDATA
GIGABYTE
DDRII CHANNEL A
GA-M61SME-S2
2.01
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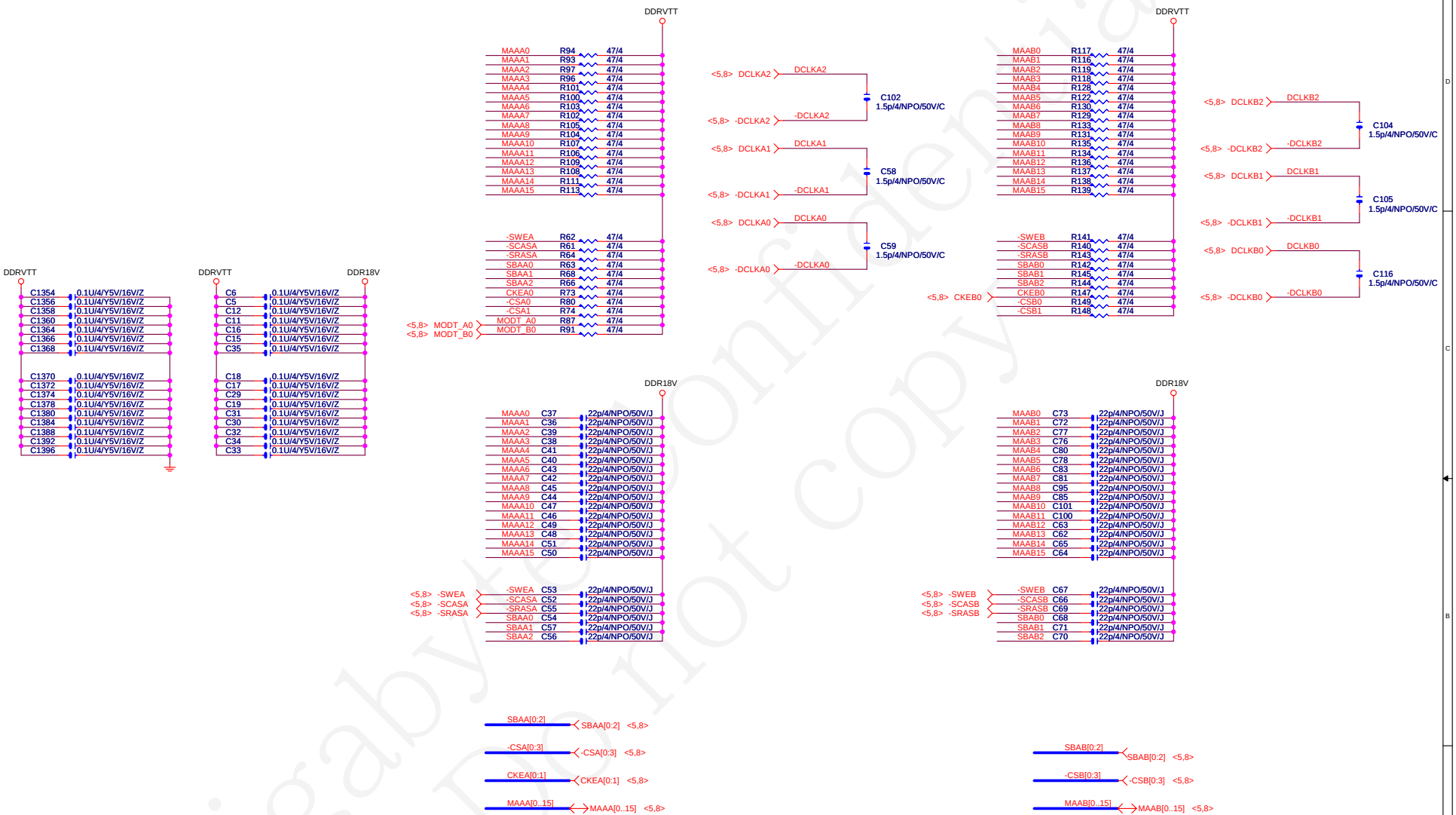

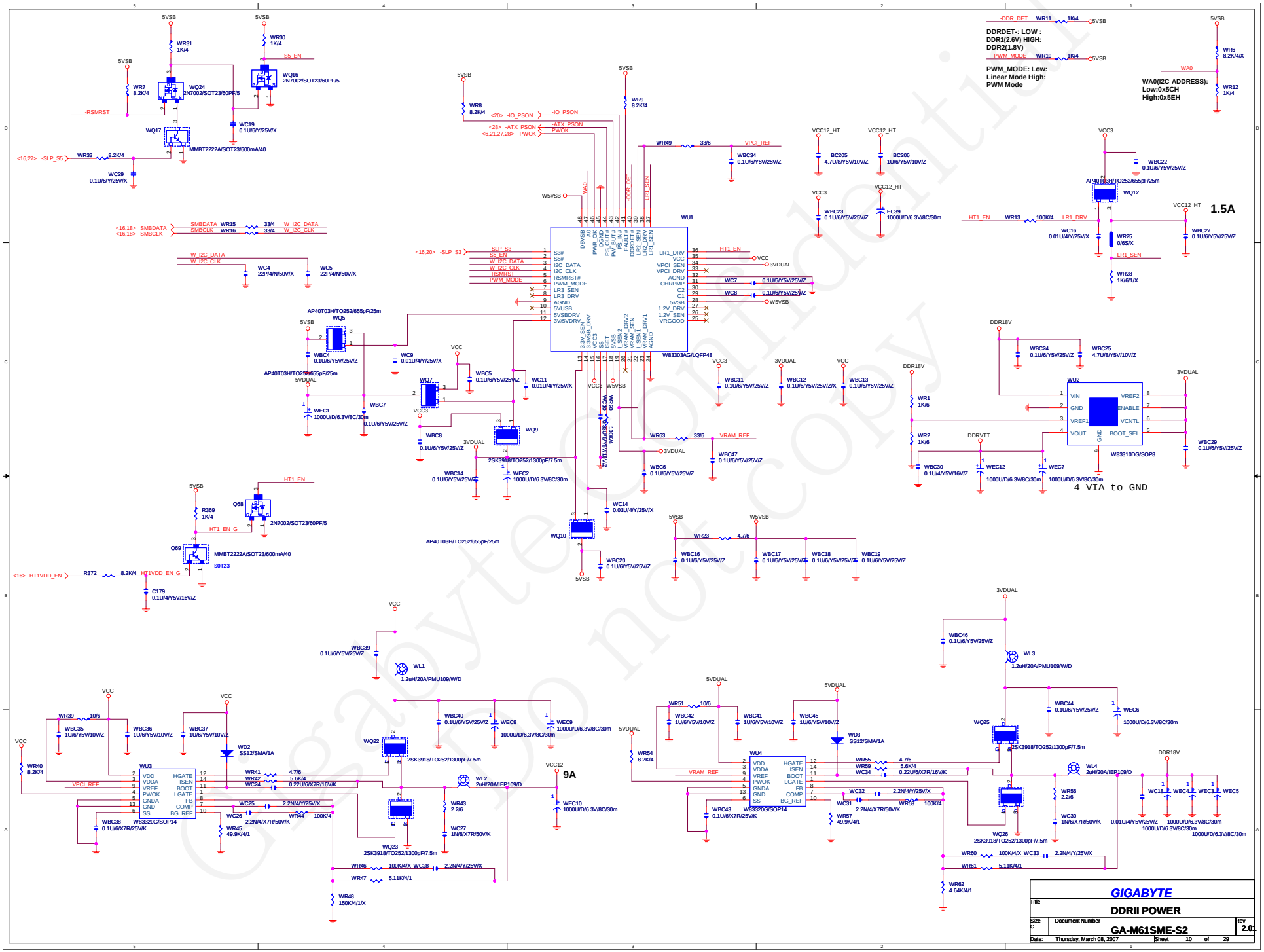
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
9A
4 VIA to GND
W83303AG/LQFP48
W83320G/SOP14
W83310DG/SOP8
GIGABYTE
DDRII POWER
GA-M61SME-S2
2.01
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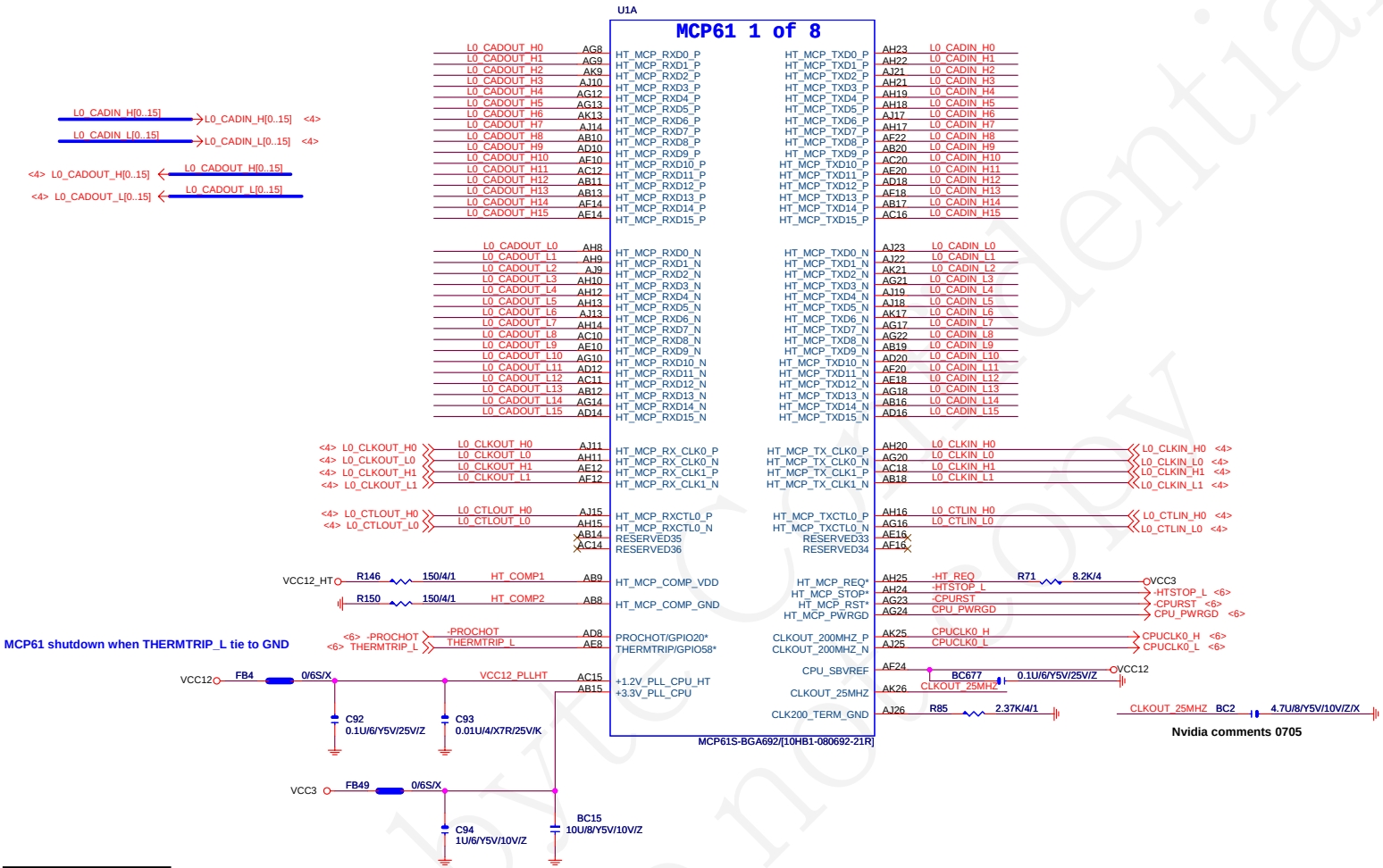

GIGABYTE			
Title	MCP61-HOST		
Size: Custom	Document Number: GA-M61SME-S2		Rev: 2.01
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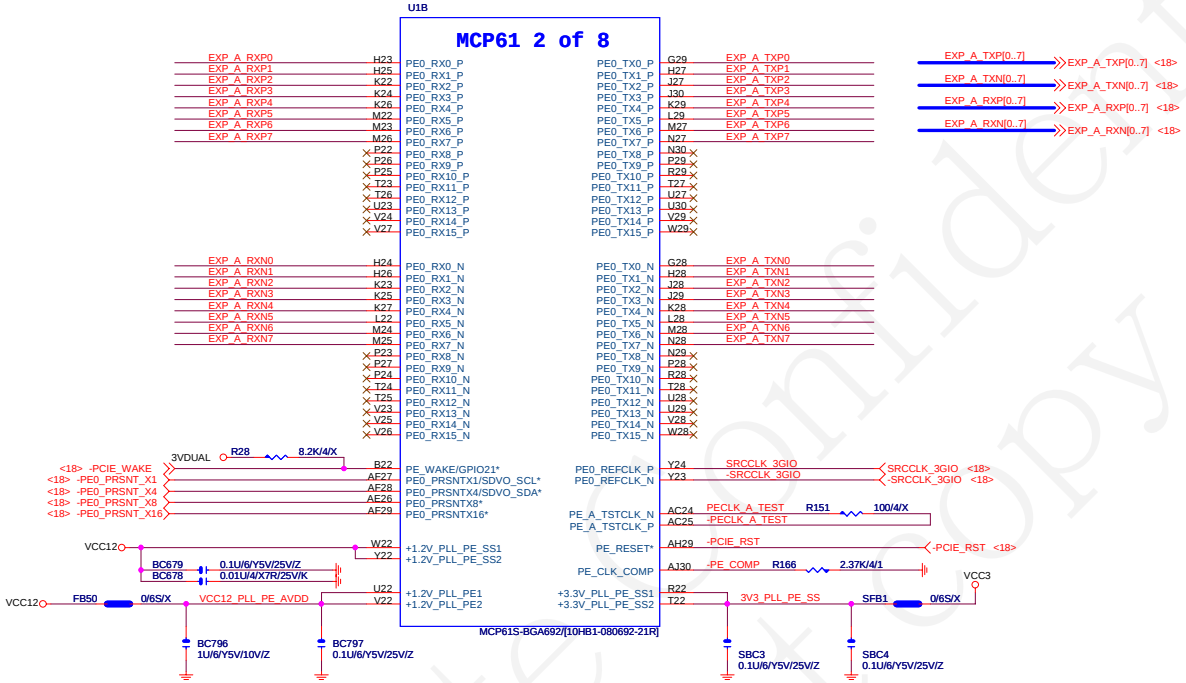

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Title: MCP61-PCI EXPRESS

Size: Custom | Document Number: GA-M61SME-S2 | Rev: 2.01

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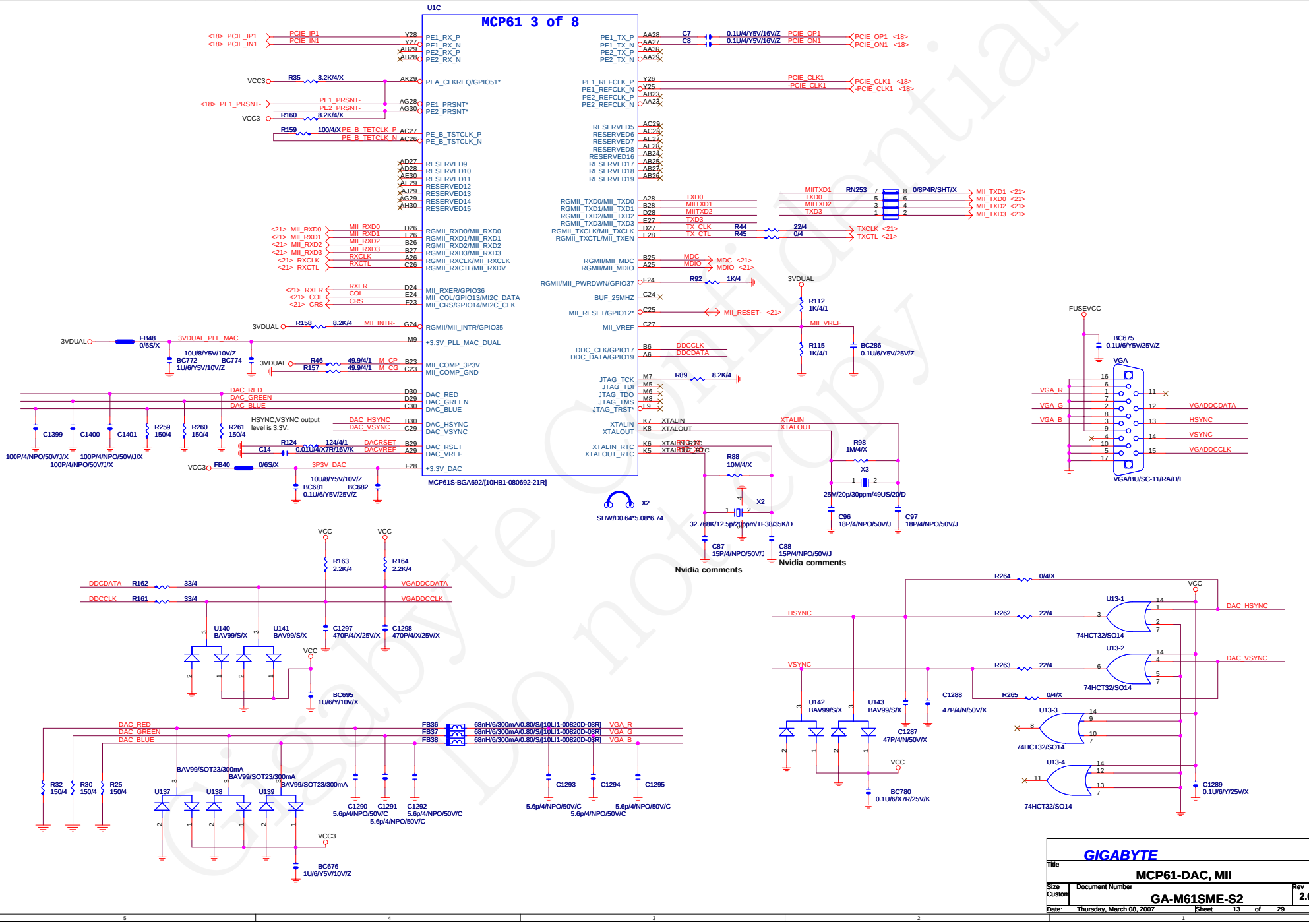

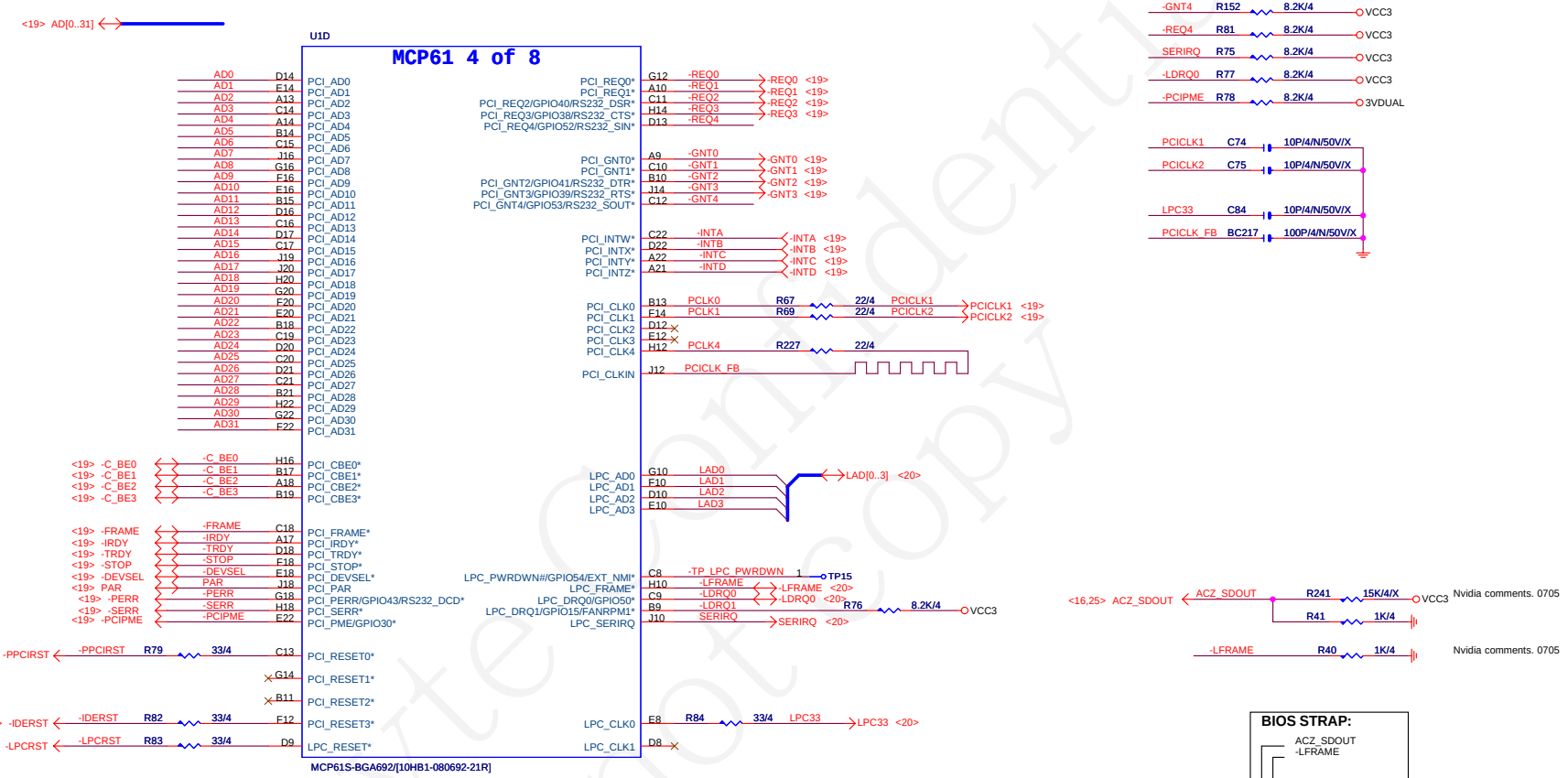

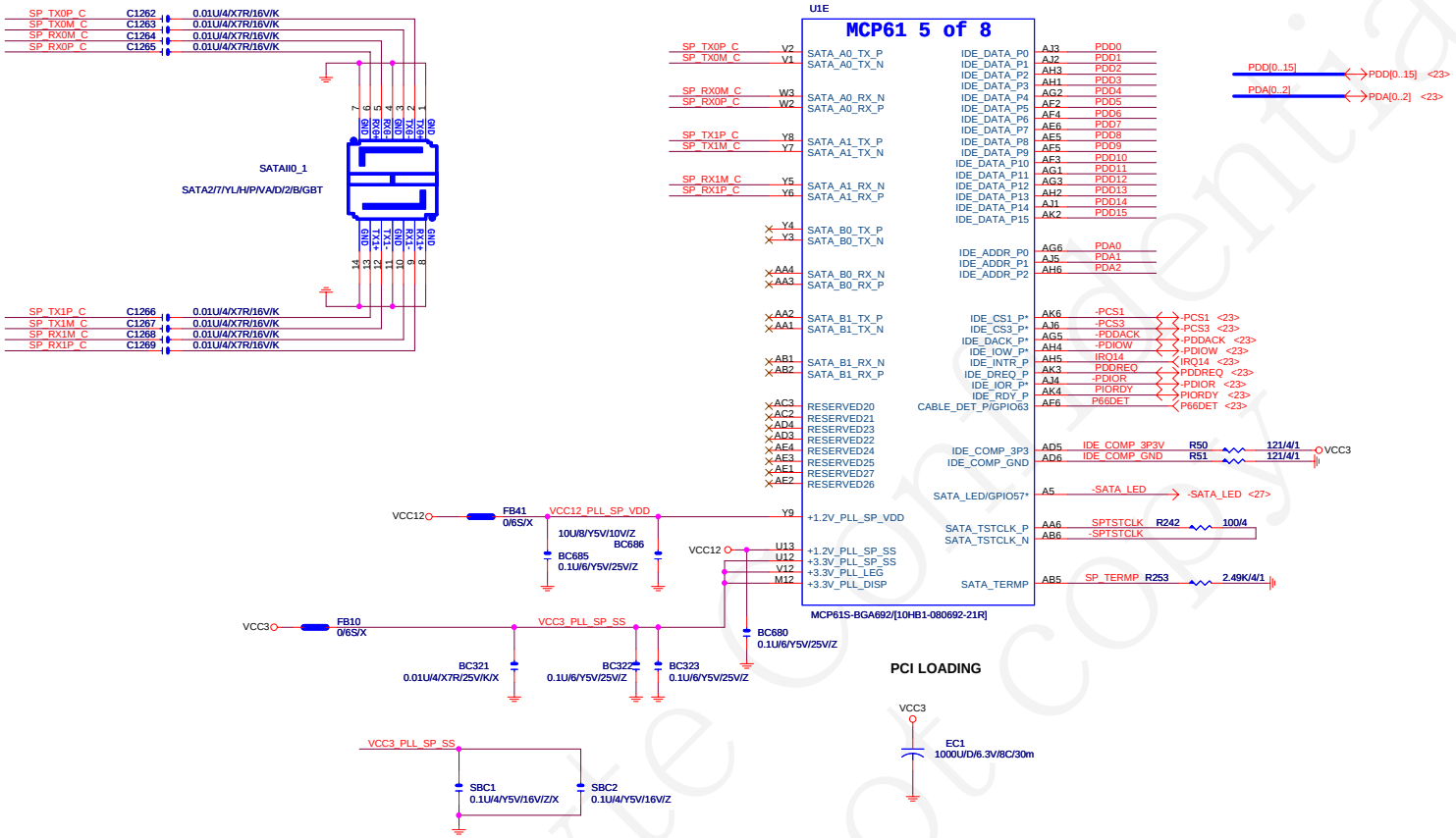

GIGABYTE

Title: MCP61-SATA/IDE

Size: Custom | Document Number: GA-M61SME-S2 | Rev: 2.01

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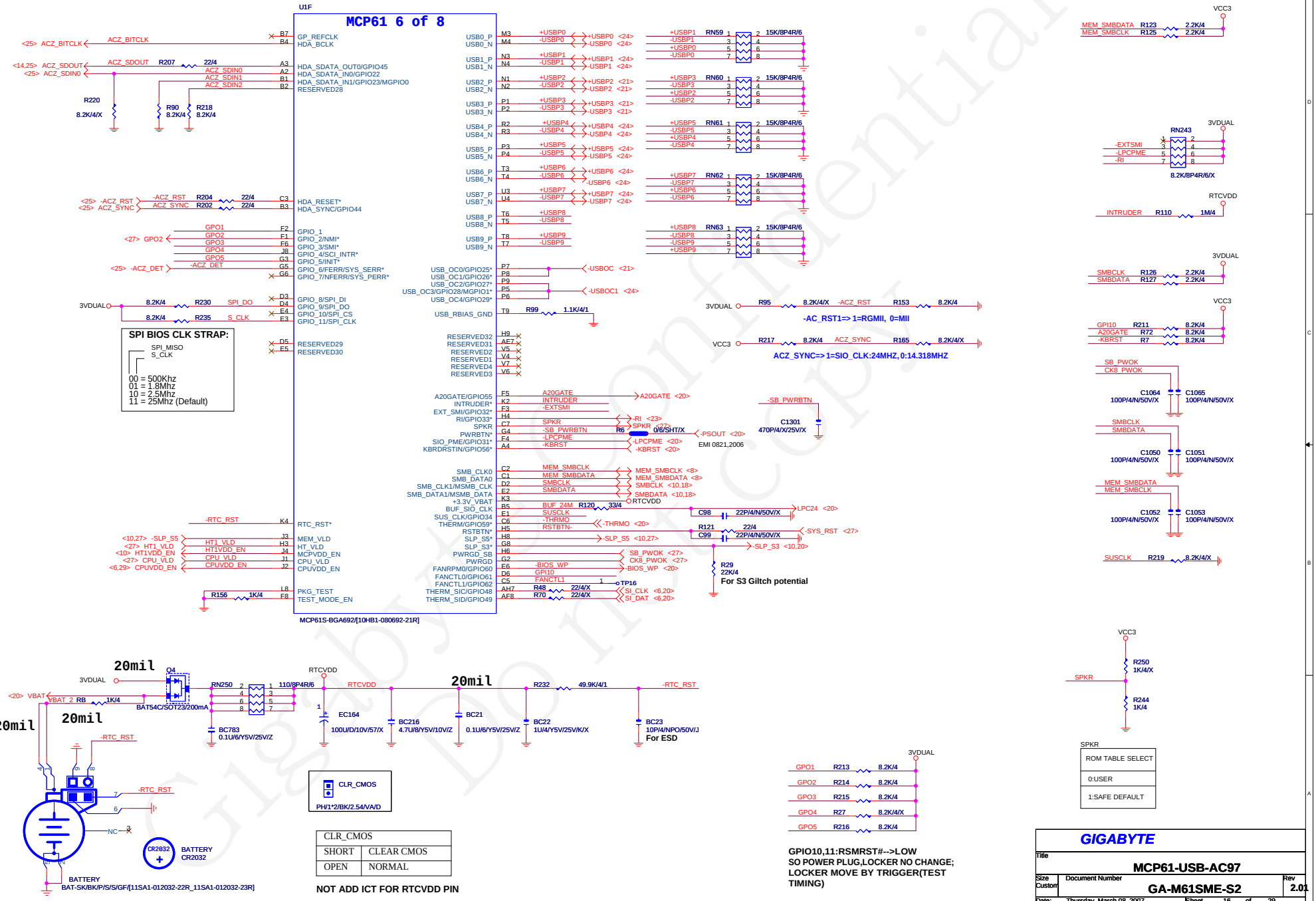
U1F
MCP61 6 of 8
MCP61S-BGA692/[10HB1-080692-21R]
SPI BIOS CLK STRAP:
SPI_MISO
S_CLK
00 = 500Khz
01 = 1.8Mhz
10 = 2.5Mhz
11 = 25Mhz (Default)
-AC_RST1=> 1=RGMII, 0=MII
ACZ_SYNC=> 1=SIO_CLK:24MHZ, 0:14.318MHZ
EMI 0821,2006
For S3 Giltch potential
For ESD
BATTERY
BAT-SK/BK/P/S/S/GF/[11SA1-012032-22R_11SA1-012032-23R]
BATTERY
CR2032
CLR_CMOS
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
GPIO10,11:RSMRST#-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST TIMING)
GIGABYTE
Title
MCP61-USB-AC97
Size Custom
Document Number
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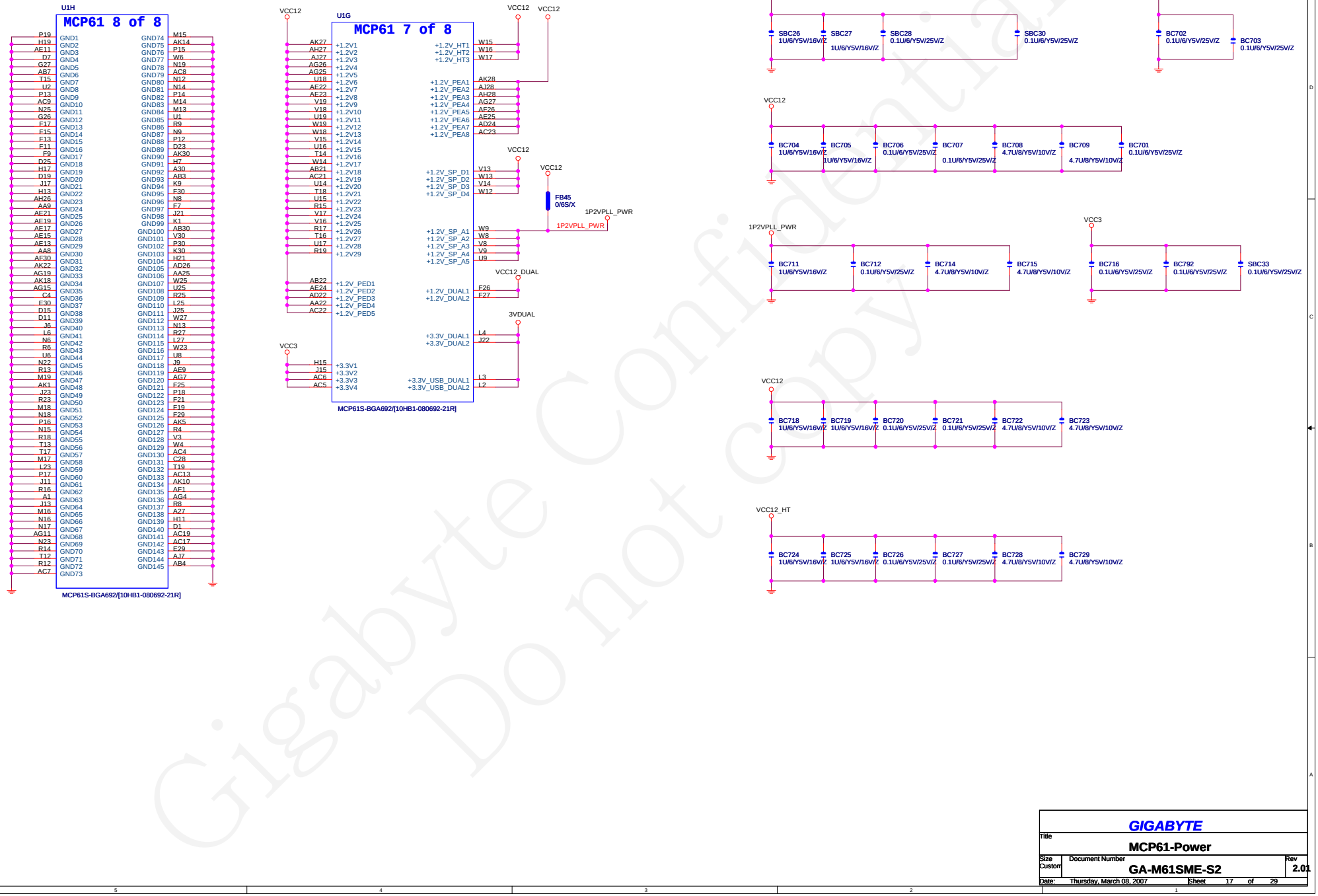

GIGABYTE

Title: MCP61-Power

Size: Custom | Document Number: GA-M61SME-S2 | Rev: 2.01

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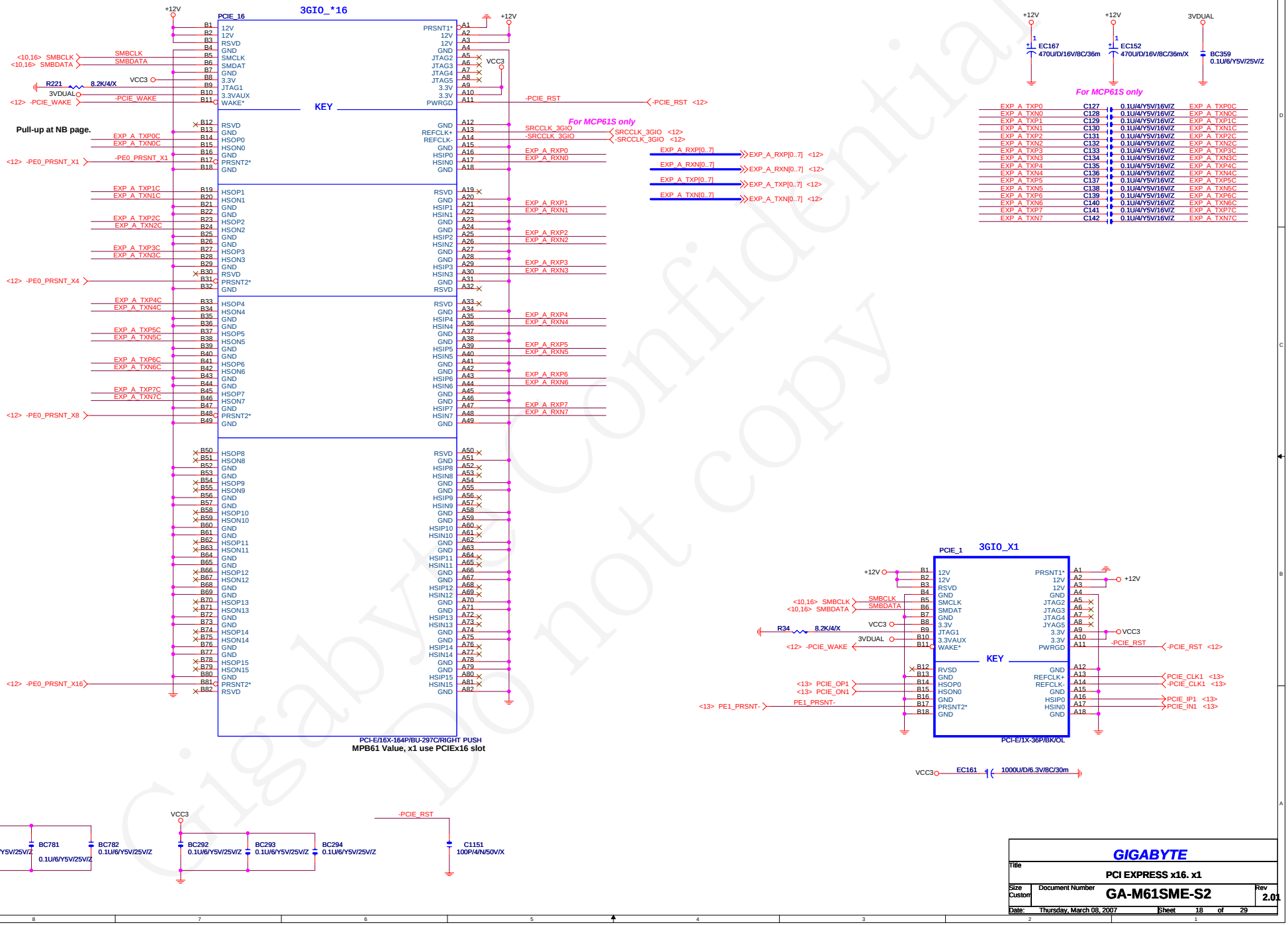

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Title	PCI EXPRESS x16. x1	
Size: Custom	Document Number: GA-M61SME-S2	Rev: 2.01
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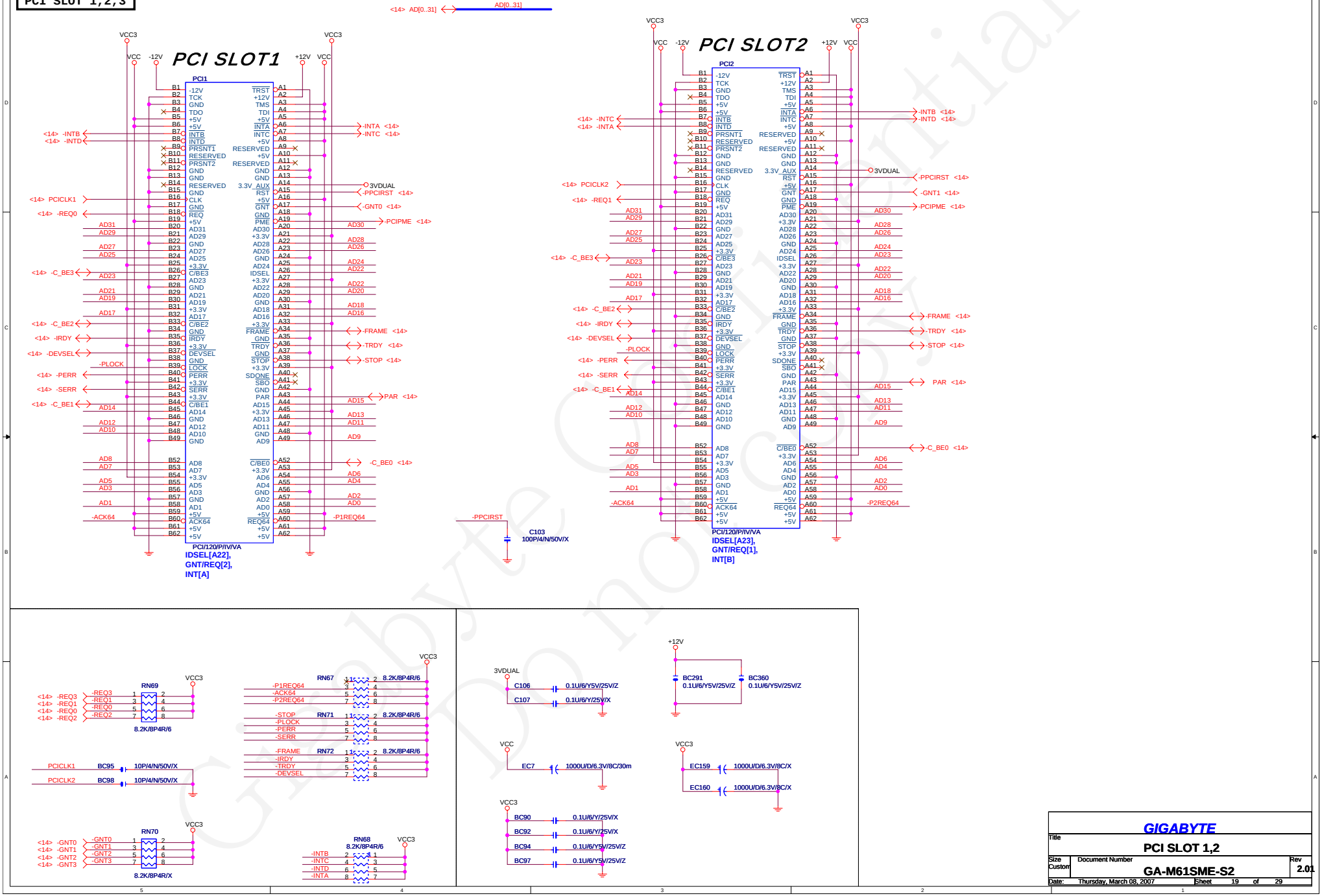
PCI SLOT 1,2,3



GIGABYTE		
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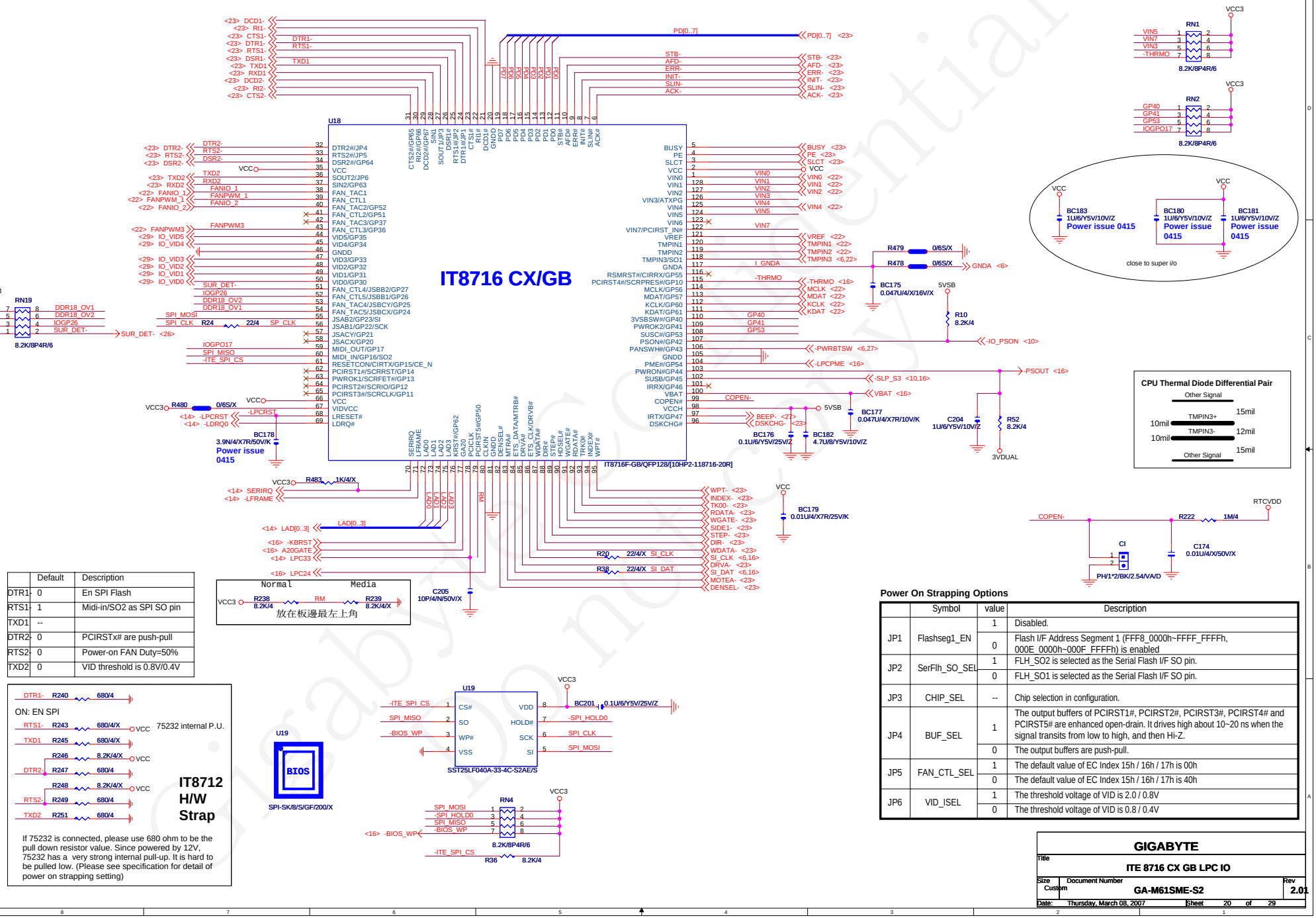


	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

ON: EN SPI

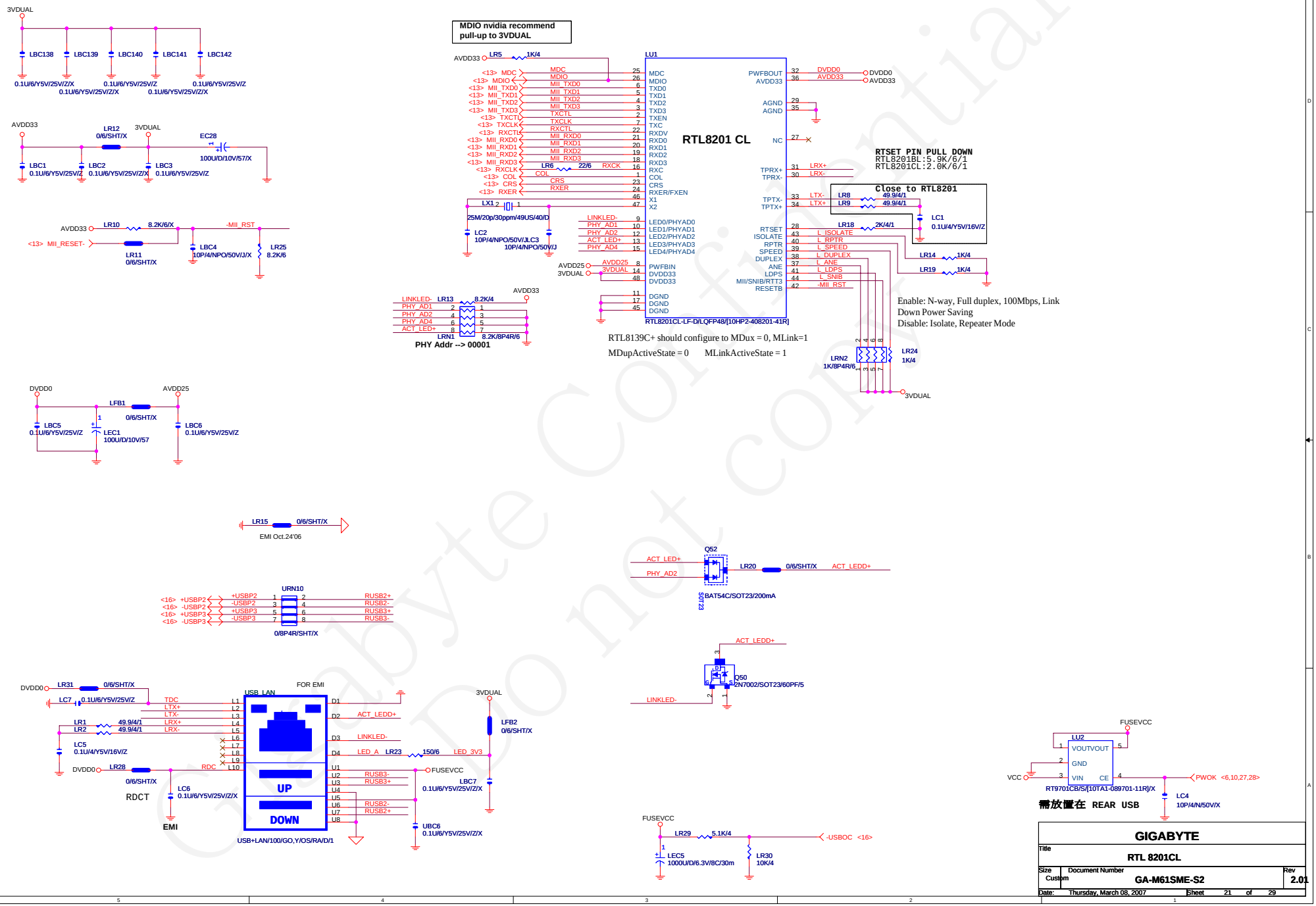
75232 internal P.U.

IT8712 H/W Strap

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V


MDIO nvidia recommend pull-up to 3VDUAL
RTL8201 CL
RTSET PIN PULL DOWN
RTL8201BL:5.9K/6/1
RTL8201CL:2.0K/6/1
Close to RTL8201
Enable: N-way, Full duplex, 100Mbps, Link
Down Power Saving
Disable: Isolate, Repeater Mode
PHY Addr --> 00001
RTL8139C+ should configure to MDux = 0, MLink=1
MDupActiveState = 0 MLinkActiveState = 1
RTL8201CL-LF-D/LQFP48/[10HP2-408201-41R]
BAT54C/SOT23/200mA
2N7002/SOT23/60PF/5
RT9701CB/S/[10TA1-089701-11RJ/X
USB+LAN/100/GO,Y/OS/RA/D/1
EMI Oct.24'06
FOR EMI
USB_LAN
UP
DOWN
EMI
RDCT
備放置在 REAR USB
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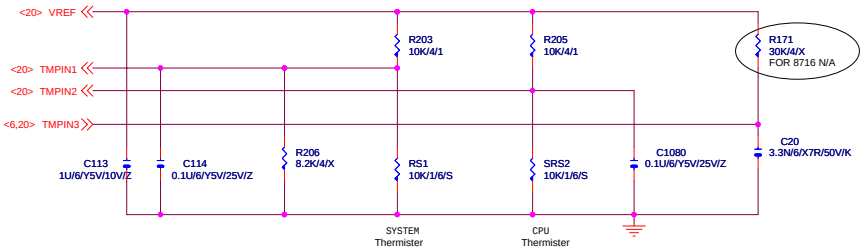
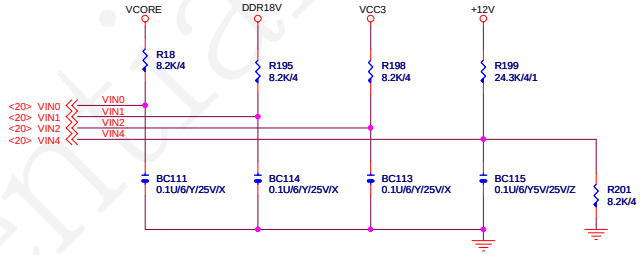
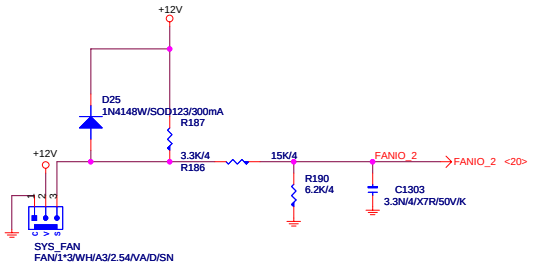
Hardware Monitor circuits

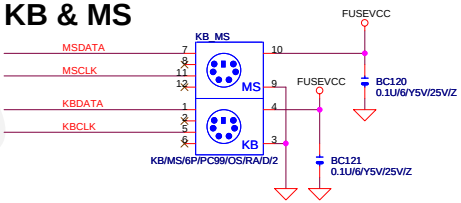


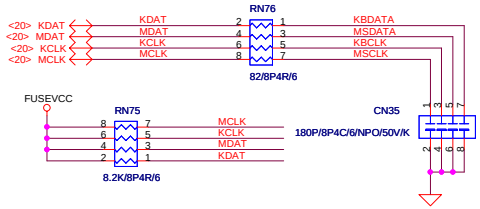


SYSTEM FAN

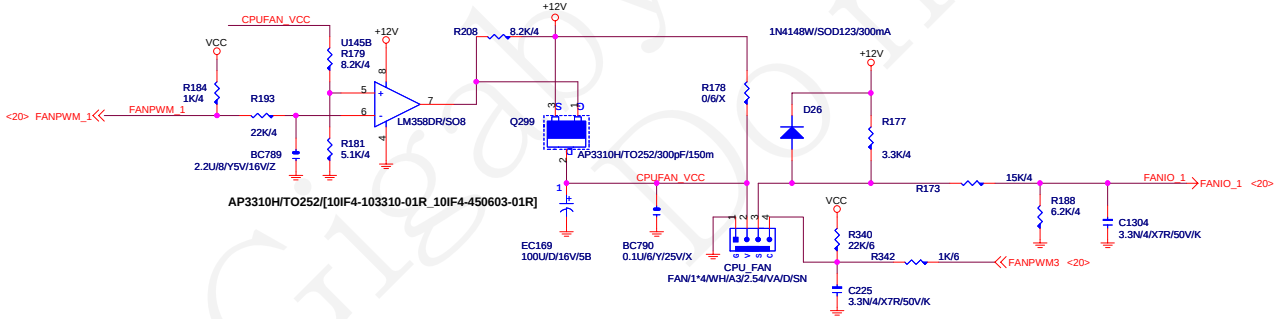


KB & MS





CPU FAN



GIGABYTE		
Title: FAN/HWMO KB/MS		
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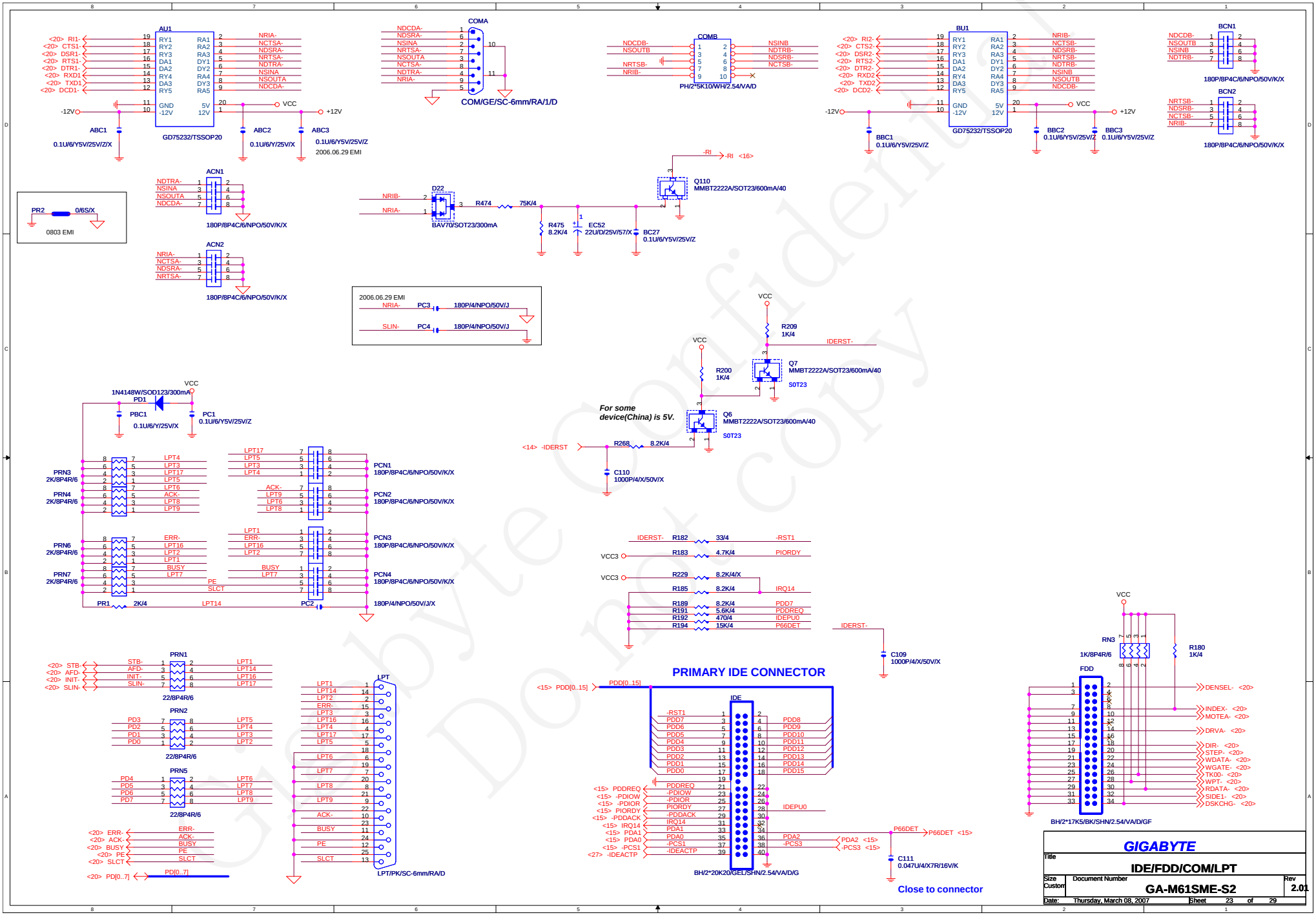

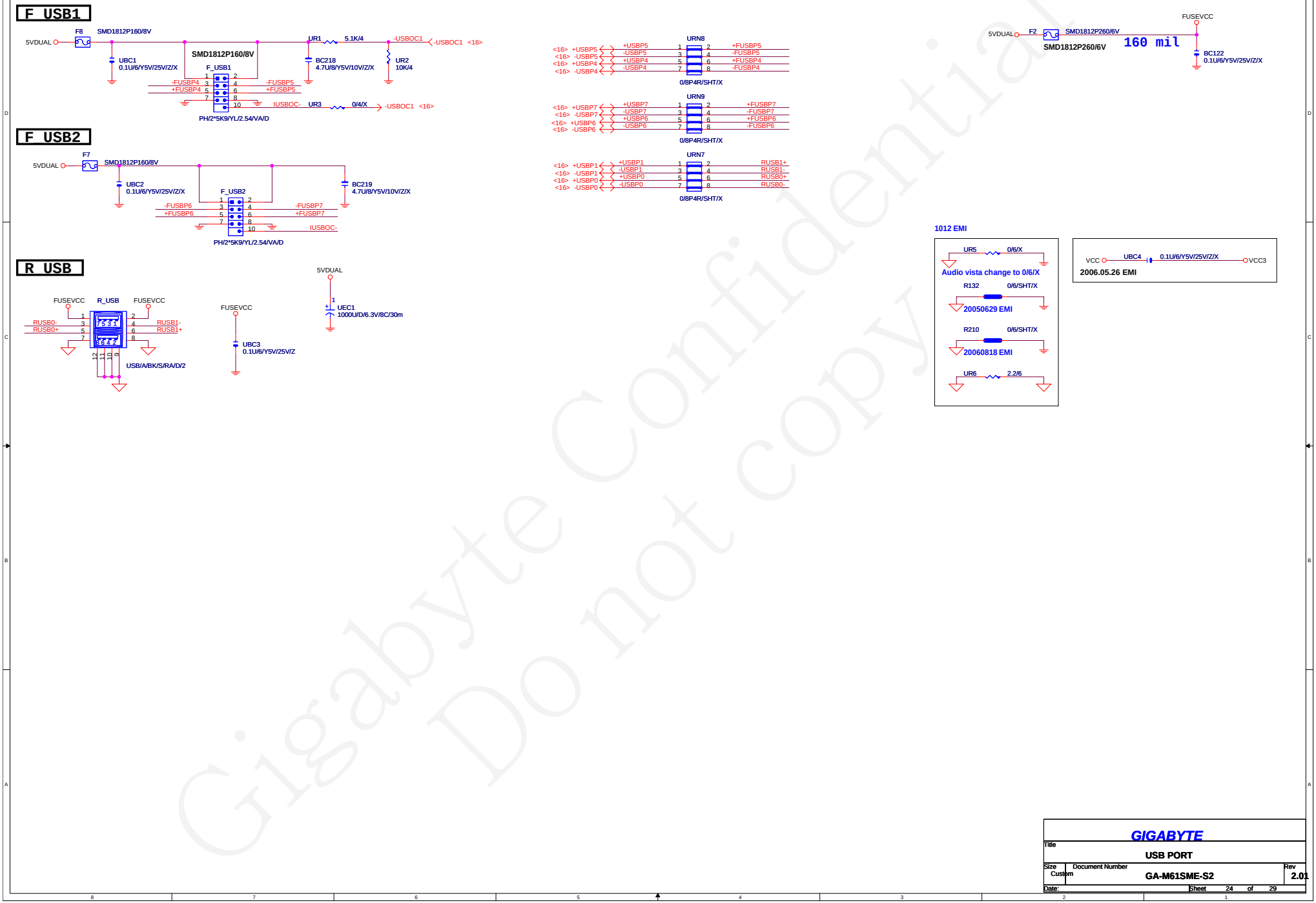

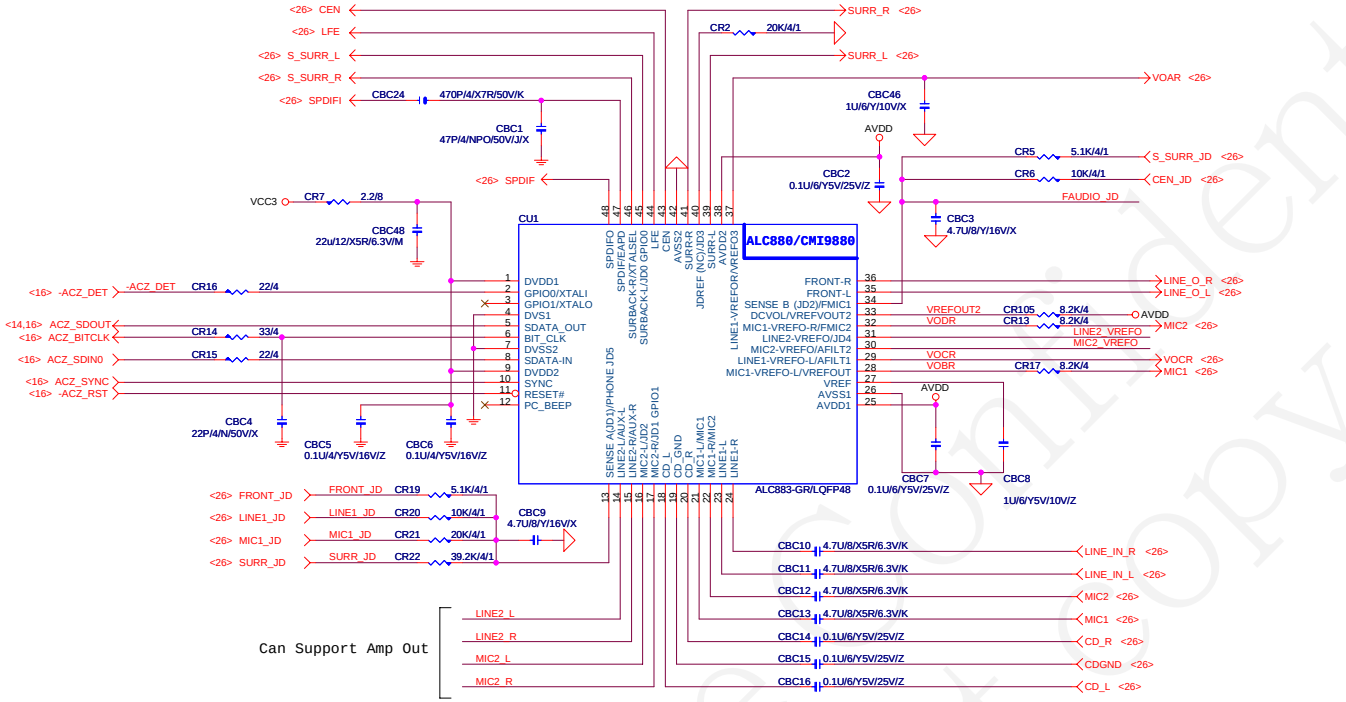

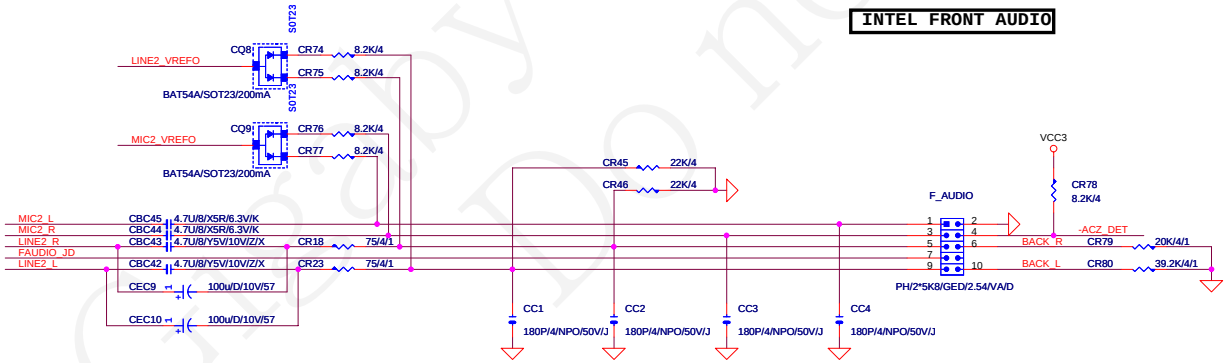

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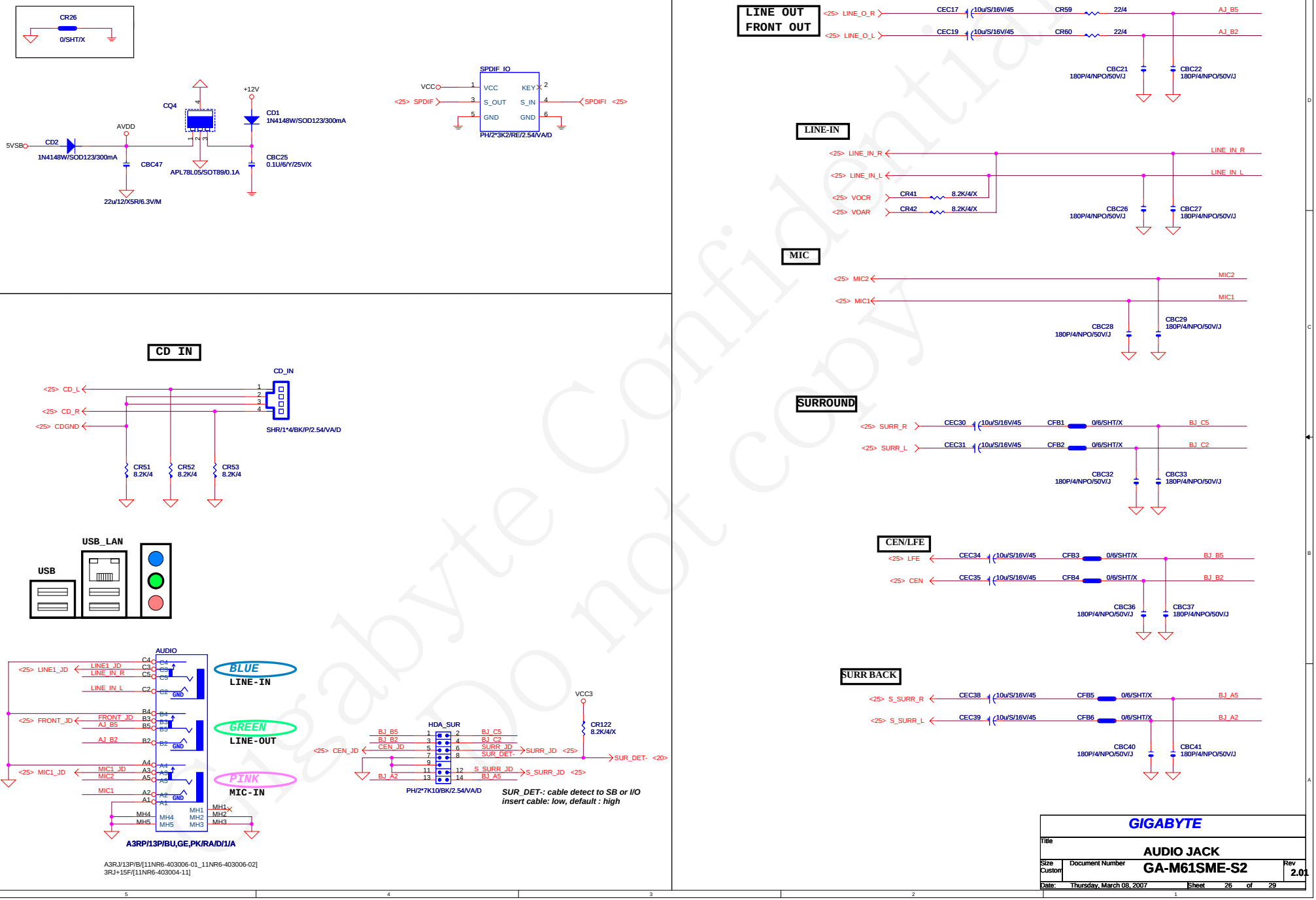
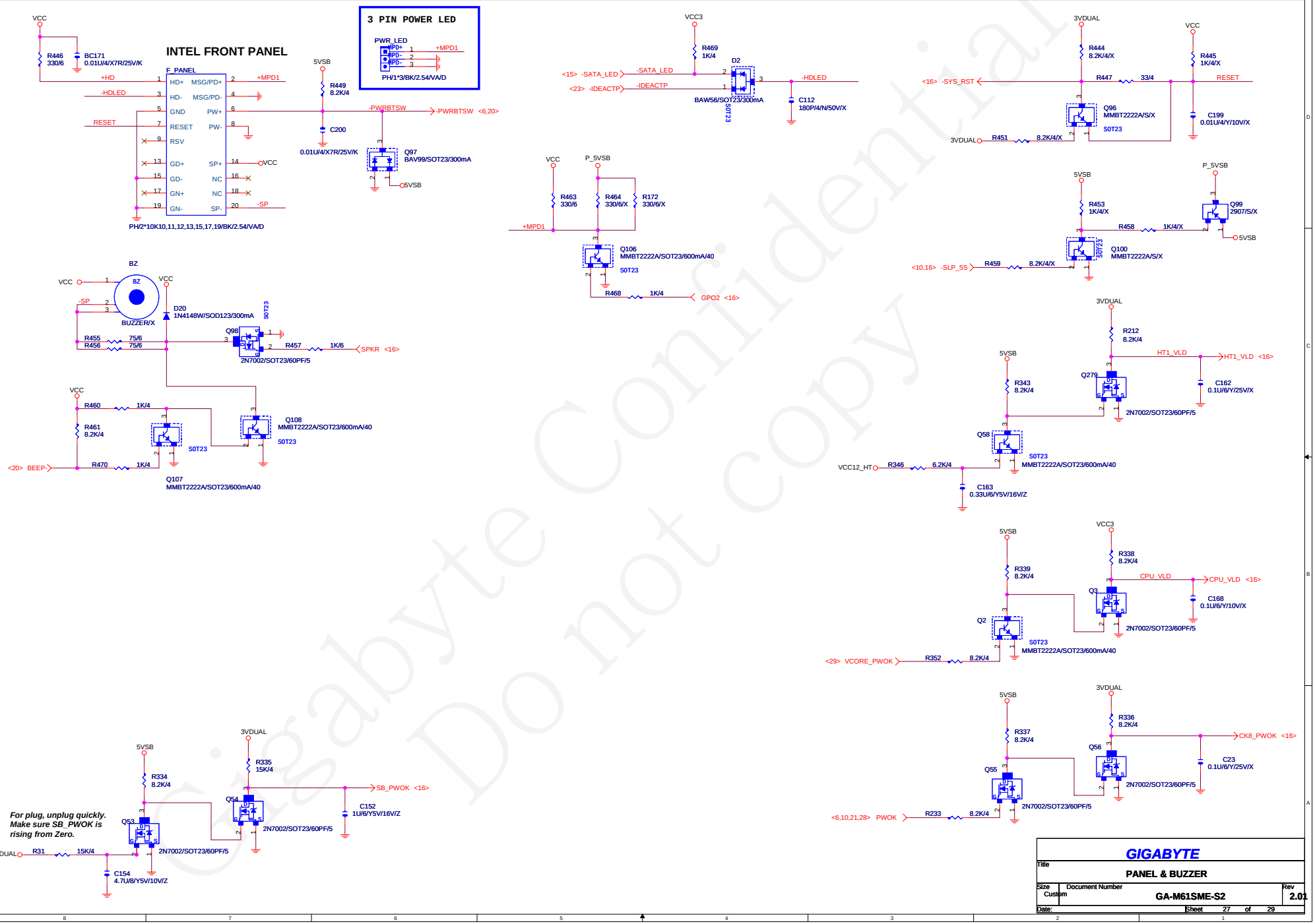
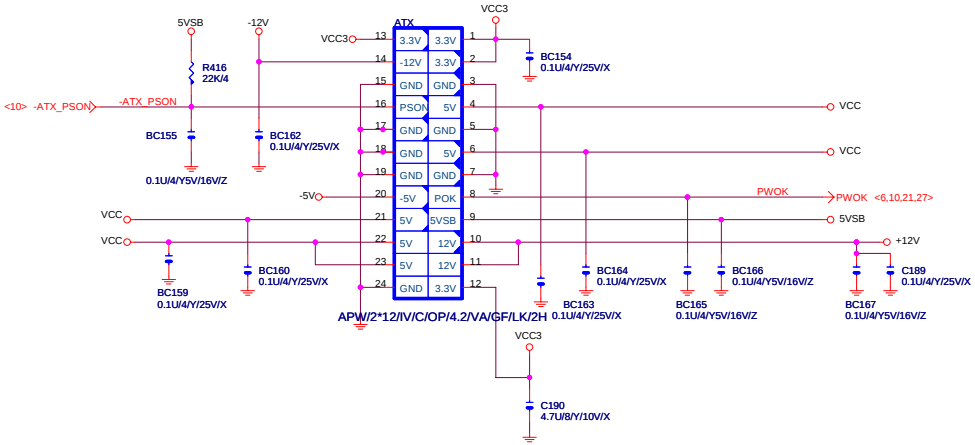
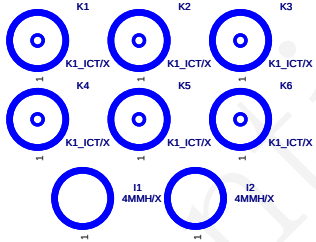
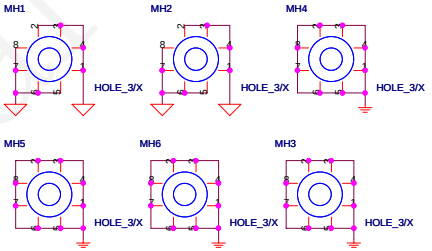


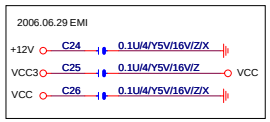


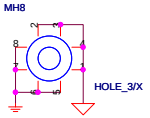
ATX POWER CONNECTOR

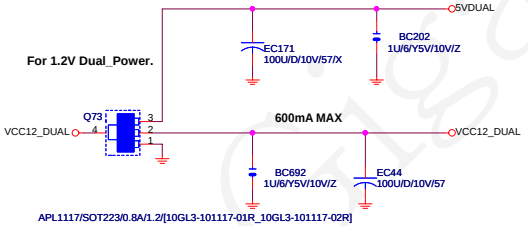


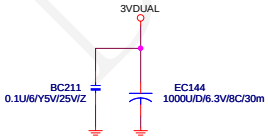


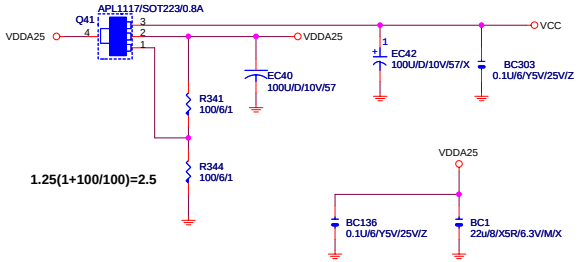












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